

## Fault Detection of 3-Phase VSI using Wavelet-Fuzzy Algorithm

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**Abstract:** The good knowledge and information about the fault mode behaviour of the PWM voltage source inverter is important to improve system design, protection and fault tolerant control. This paper develops a real-time condition-monitoring algorithm for 3-phase pulse width modulation (PWM) inverter in fuzzy speed controlled induction machine. It is designed to detect and identify the transistor open-circuit fault and an intermittent misfiring fault, which commonly occurs in the inverter drive system. The condition monitoring mechanism is based on discrete wavelet transform (DWT) and fuzzy logic (FL). In this method, the stator currents are used as an input to the system. No direct access to the induction motor is required. The developed system has been rigorously assessed theoretically and experimentally, and it has been shown that the system is robust and reliable.

**Key words:** System design, fault tolerant control, condition monitoring mechanism, fuzzy logic

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### INTRODUCTION

With the development of power electronics, microprocessor and digital signal processor (DSP), induction motors are predominantly fed from pulse width modulation (PWM) inverters for variable-speed operation. PWM inverter fed motors are usually more reliable than those supplied directly on-line. For example, the problem of broken rotor bars, mainly due to excessive starting torque, is practically avoided by technique of soft starting with an inverter<sup>[1]</sup>.

However, a previous study of three-phase voltage-fed inverter demonstrated that they can also develop various faults which is preventing their wide spread application<sup>[2,3]</sup>. These faults can lead to motor failure if left undetected. As we all aware, motor problems can cause crises that are expensive and quite annoying, in particular, if the problem could be prevented<sup>[4]</sup>.

To solve this problem, the condition monitoring and fault detection of voltage source inverter (VSI) is necessary. Condition monitoring, fault detection and diagnosis system allow preventive and condition-based maintenance to be arranged for the system during scheduled downtime. This will prevent an extended period of downtime caused by extensive machine failures, which will improves the overall availability and performance, while reducing maintenance costs<sup>[5]</sup>.

Condition monitoring means the continuous assessment of the performance and health of the system throughout its useful operating life. Diagnosis, though,

is a special case of the more general problem of condition data interpretation, as it sets out to determine the source of any abnormality in the data, based on a given set of possible cause and effect symptoms. The aim of diagnosis is: based on a minimum amount of input data, using the minimum and simplest analysis, to determine and isolate as fast as possible, the cause of any inadequate performance or any actual equipment failure.

This paper present detail practical results on condition monitoring of pulse width modulation (PWM) voltage source inverter (VSI) for closed-loop, fuzzy logic v/f speed control strategy of an induction motor drive, as shown in Fig. 1. A combination of discrete wavelet transform (DWT) and fuzzy logic (FL) is proposed to detect and identify the transistor open-circuit fault and an intermittent misfiring fault. These typical true faults can lead to catastrophic breakdown of the motor if left undetected. Continuous monitoring for such condition is absolutely importance since these types of faults wouldn't trigger the circuit protection device.

**Fault Identification:** To operate power transistors such as MOSFET or IGBT, an appropriate gate voltage must be applied in order to drive transistors into the saturation mode for low on-state voltage. Malfunctioning of gate drive circuit can lead to the transistor base drive open-circuit fault.

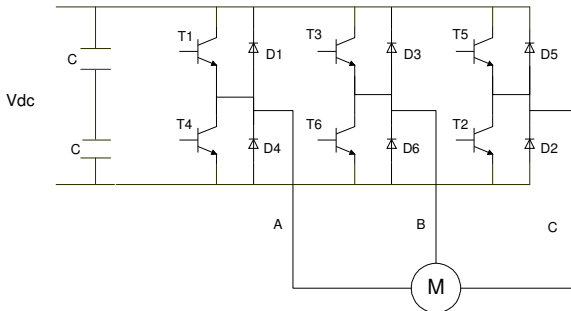


Fig. 1: A PWM voltage-fed inverter of induction motor drive

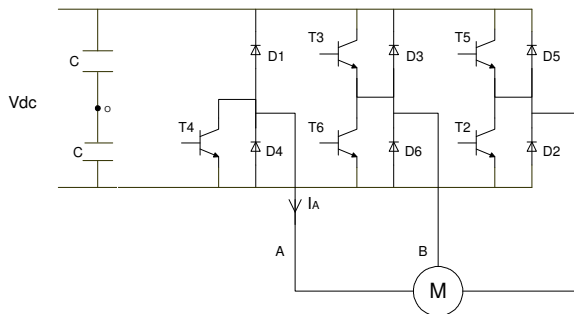


Fig. 2: Equivalent circuit of inverter after the fault occurrence

Since the transistor T1 has now an open-circuit fault, the phase A of the induction machine is connected to the positive dc rail through the diode D1, as presented in Fig. 2. The machine phase A voltage is then determined by the polarity of current and the switching pattern of transistor T4. The phase voltage ( $V_A$ ) will be clamped to the negative rail if stator current phase A, ( $i_A$ ) is positive. On the other hand, the phase voltage  $V_A$  will be clamped to the negative rail when transistor T4 is switch on, and then to the positive rail when transistor T4 is off and D4 is on, if  $i_A$  is negative.

This fault situation can be clearly described by Algorithm A below<sup>[6]</sup>. It is expressed in terms of commands if (premises), and/or (logical operation), then (conclusion) and else if (alternatives). In that algorithm,  $\pm v_{dc}/2$  is the dc-link voltage, VAO is the pole voltage of phase A and  $T4 = 0$  and  $T4 = 1$  correspond to the opened switch and closed switch, respectively.

**Algorithm A Phase Voltage A after the fault occurrence:**

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If  $i_A > 0$  then
 $\Rightarrow VAO = -v_{dc}/2$ 
else if  $i_A < 0$  and  $T4 = 1$  then
 $\Rightarrow VAO = -v_{dc}/2$ 
else if  $i_A < 0$  and  $T4 = 0$  then
 $\Rightarrow VAO = v_{dc}/2$ 
end if
    
```

The phase currents will be balanced and sinusoidal with a dc offset after the fault because the phase

voltages ( $V_A, V_B, V_C$ ) are balanced with the sinusoidal pwm modulation before and after the fault. The dc offset current in phase A will be equally divided between the phase B and phase C and worsen the current stress of the switching devices in phases B and C.

If the inverter system is connected to the induction motor, the maximum average torque capability of the drive is substantially reduced because the dc offset will produce a braking torque. Also, interaction between the dc offset component of the stator flux and the fundamental frequency rotor current will cause fundamental frequency pulsating torque that can be particularly harmful at low operating frequency and low shaft inertia. This conclusion is only valid under the assumption of magnetic linearity and infinite rotor inertia.

**Proposed scheme:** Figure 3 shows the flowchart of the fault detection scheme proposed. The process can be divided into three main stages: detection, feature extraction and fault identifier. The development of proposed scheme that is based on wavelet transform and fuzzy logic.

**Change detection of stator currents:** A change in stator current waveform is defined as the instant at which a sudden increases, decreases or transients are observed in the magnitude of the current. Thus, the application of the wavelet analysis is well suited. The wavelet transform provides a good means of studying how the frequency content changes with time and consequently is able to detect and localise short-duration malfunctions<sup>[7]</sup>.

In this paper, a discrete wavelet transform (DWT) is used to detect the change with the aid of a 'sliding data window'<sup>[8]</sup>. The window slide across the current waveforms by a time step of 3 ms while capturing 30 ms segment of the waveform at each time step. At each time step, the data in the window is fed to the DWT to compute the corresponding DWT coefficients. A change is considered to have occurred in the stator current waveforms if any wavelet coefficient exceeds or falls below a given band. On detecting the current waveform change, the sliding data window aligns itself to the point when the change was detected. Then, the DC offset in the currents is calculated before feeding them to the fuzzy logic system.

**Fault identifier:** The fault identifier process by fuzzy logic system leads to the determination of particular faults, which was occurred in the system. This process takes place after a system checked the status of stator currents. The currents need to be checked to ensure that all three-phase currents are connected to the system. Otherwise, the fuzzy system will prompt a single phasing fault.

Table 1: If – Then rules

| Rules | If               |   |      | Then |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |   |
|-------|------------------|---|------|------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|---|
|       | -DC              | Z | + DC | G    | T <sub>1if</sub> | T <sub>2if</sub> | T <sub>3if</sub> | T <sub>4if</sub> | T <sub>5if</sub> | T <sub>6if</sub> | T <sub>1of</sub> | T <sub>2of</sub> | T <sub>3of</sub> | T <sub>4of</sub> | T <sub>5of</sub> | T <sub>6of</sub> |   |
| 1     | I <sub>ADC</sub> | √ |      |      |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |   |
|       | I <sub>BDC</sub> |   | √    |      | √                |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |   |
|       | I <sub>CDC</sub> |   | √    |      |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |   |
| 2     | I <sub>ADC</sub> | √ |      |      |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |   |
|       | I <sub>BDC</sub> |   |      | √    |                  | √                |                  |                  |                  |                  |                  | √                |                  |                  |                  |                  |   |
|       | I <sub>CDC</sub> |   |      | √    |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |   |
| 3     | I <sub>ADC</sub> |   |      | √    |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |   |
|       | I <sub>BDC</sub> | √ |      |      |                  |                  | √                |                  |                  |                  |                  | √                |                  |                  |                  |                  |   |
|       | I <sub>CDC</sub> |   |      | √    |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |   |
| 4     | I <sub>ADC</sub> |   |      | √    |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |   |
|       | I <sub>BDC</sub> | √ |      |      |                  |                  | √                |                  |                  |                  |                  |                  |                  | √                |                  |                  |   |
|       | I <sub>CDC</sub> |   |      | √    |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |   |
| 5     | I <sub>ADC</sub> |   |      | √    |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |   |
|       | I <sub>BDC</sub> | √ |      |      |                  |                  |                  | √                |                  |                  |                  |                  |                  |                  | √                |                  |   |
|       | I <sub>CDC</sub> | √ |      |      |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |   |
| 6     | I <sub>ADC</sub> |   |      | √    |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |   |
|       | I <sub>BDC</sub> |   |      | √    |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | √                |   |
|       | I <sub>CDC</sub> | √ |      |      |                  |                  |                  |                  |                  | √                |                  |                  |                  |                  |                  |                  |   |
| 7     | I <sub>ADC</sub> | √ |      |      |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |   |
|       | I <sub>BDC</sub> |   |      | √    |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | √ |
|       | I <sub>CDC</sub> | √ |      |      |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |   |

Note:

I<sub>ADC</sub> = DC offset of phase A    VM = Inverter condition    Tif = Transistor intermittent misfiring fault  
 I<sub>ABC</sub> = DC offset of phase B    G = Good condition    Tof = Transistor open-circuit fault  
 I<sub>CDC</sub> = DC offset of phase C    Z = Zero DC offset    +DC = Positive DC offset

-DC = Negative DC offset

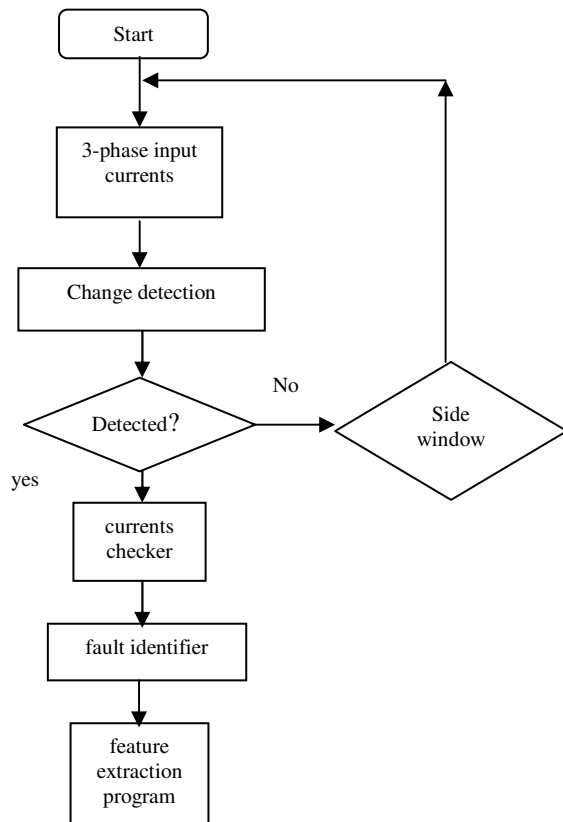


Fig. 3a: Flowchart of fault detection process

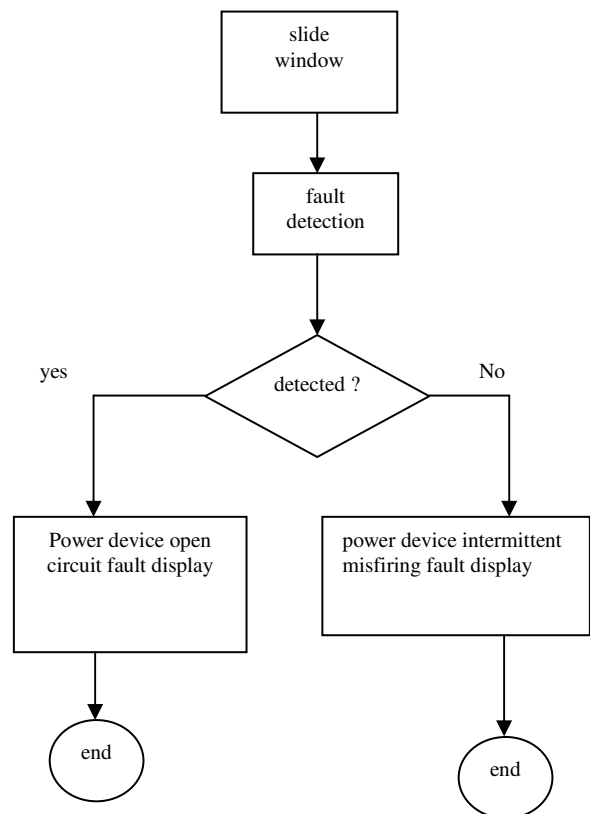


Fig. 3b: Flowchart of feature extraction program

On detecting fault, the system will calculate the value of DC offset in the currents. The value and polarity of the DC offset is then fed to the fuzzy logic system to determine the faults. Fuzzy logic algorithms adopted in the proposed fault identifier are systematically designed according to intuition and experiences about the 3-phase VSI behaviour. The advantage of using the fuzzy logic is that it is easy to apply heuristics knowledge and 'rule-of-thumb' experience. In this project, the level of DC offset of all three stator currents are considered as the variables to the fuzzy system.

To identify the faults is not always straightforward case, particularly when in practice, the signal always containing noise and disturbance. For instance, a slight load unbalance during normal operation may introduce a low level DC offset on one of the phase currents. Measurement and sensor errors may also give misleading information. To exclude such cases from faulty operation category, fuzzy rules should be carefully designed.

Fuzzy rules and membership functions are constructed by observing the input data set. For the measurements related to the stator currents DC offset, more insight into the data is required. Therefore, membership functions will be generated for zero, DC offset positive (+DC) and DC offset negative (-DC). For the measurement related to VSI condition, it is necessary to know if the VSI is in good condition (G), switching device intermittent misfiring fault ( $T_{1if}$ ,  $T_{2if}$ ,  $T_{3if}$ ,  $T_{4if}$ ,  $T_{5if}$ ,  $T_{6if}$ ), or power device base open-circuit fault ( $T_{1of}$ ,  $T_{2of}$ ,  $T_{3of}$ ,  $T_{4of}$ ,  $T_{5of}$ ,  $T_{6of}$ ).

Once the form of the initial membership functions has been determined, Fuzzy If-Then rules can be derived. The rules for this proposed VSI fault diagnosis algorithm is shown in Table 1.

**Feature extraction:** The feature extraction process, as shown in Fig. 3b is introduced to enhance the difference between the transistor base drive open-circuit fault and an intermittent misfiring of inverter switching devices. The process takes place only after a fault detected by FLS in the stator current waveforms. On detecting and identifying the fault, the system will wait for few cycles before checking the fault for the second time. The transistor base drive open-circuit fault is considered to have happened if the DC offset still exists in the stator currents. However, if the DC offset is found to be zero or near zero in the later event, the intermittent is considered to have happened. In case of intermittent misfiring, the currents normally take a few cycles to settle back to normal operating condition, depending on drive controller type<sup>[9]</sup>.

## RESULTS

The motor used in this experiment is a 3-phase, 50 Hz, 3 hp, 4 pole, squirrel cage induction motor. The PWM waveform waveforms and the fuzzy controller are performed on a single chip Intel 80C196KC 16-bit

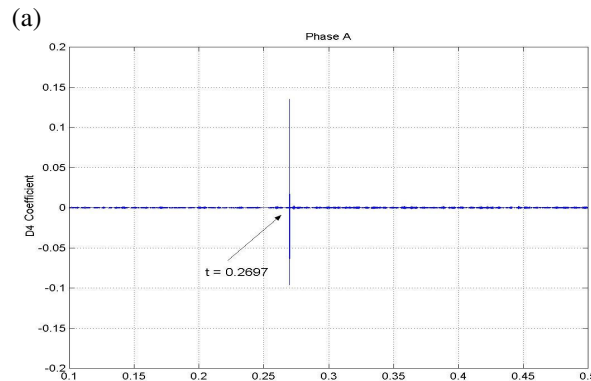
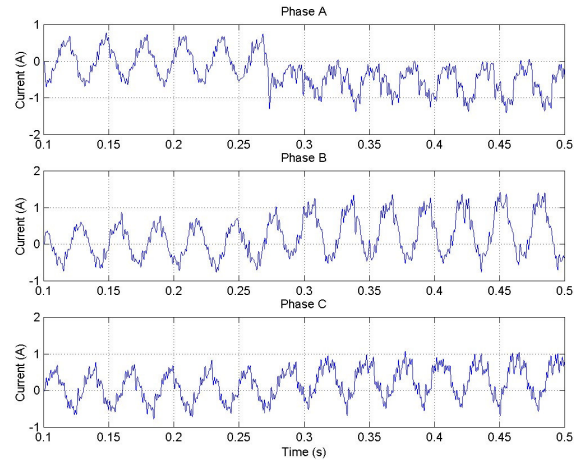
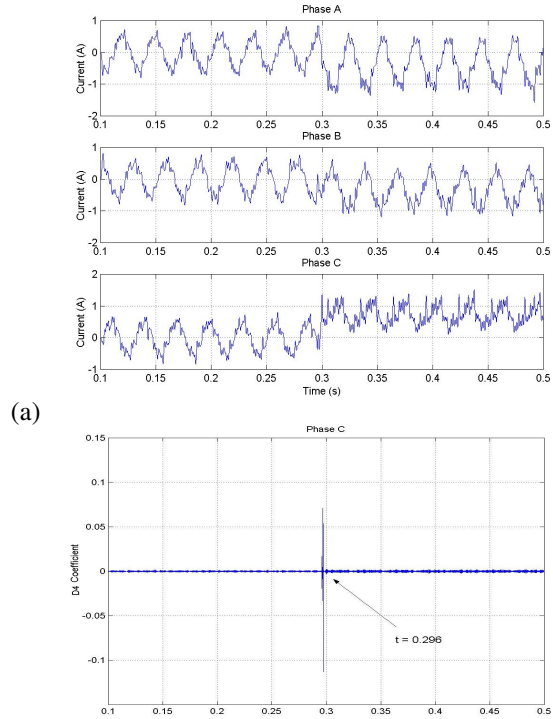


Fig. 4: The experimental result of transistor T1 open-circuit fault. (a) Stator current waveforms during transient, (b) The D4 coefficient of phase A

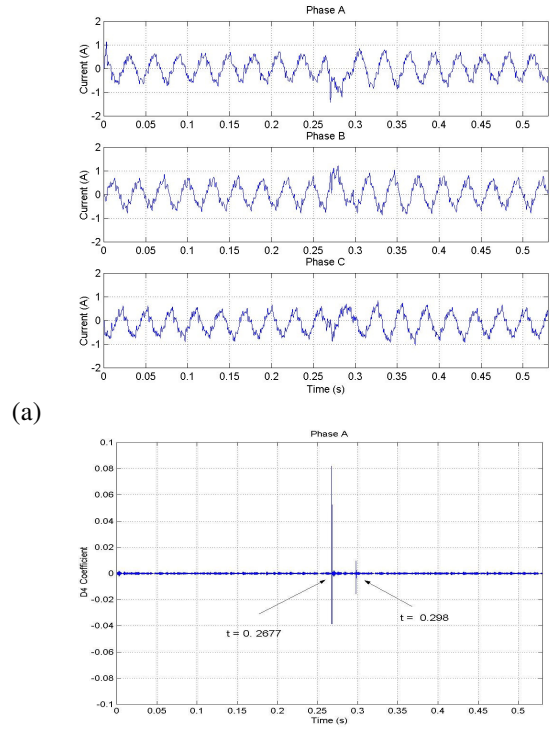
micro controller. The motor shaft is coupled with a dc generator. The drive system was initially tested under the normal operation mode. The speed was kept constant at 1000 rpm with 100V dc supply.

Then, the first fault, which is the transistor base drive open-circuit fault, is introduced and stator currents are examined as a function of failure mode. Figure 4-6 show the stator currents and DWT coefficient of T1, T2 and T3 open-circuit fault, respectively. It should be noted that this fault introduced the dc offset to the phase currents, as can be clearly seen. A larger dc offset magnitude is detected in faulty phase, as compared to the other phases. Also, the polarity of dc offset in faulty phase is opposite with the other phases. No doubt, the DWT is able to capture the significant irregular data pattern such as sharp "jumps" in current waveforms, as clearly observable in DWT coefficient. The wavelet is localised in time. This feature is important to determine the exact instant when the fault is occurred. Here is a noteworthy example of an advantage of DWT analysis.

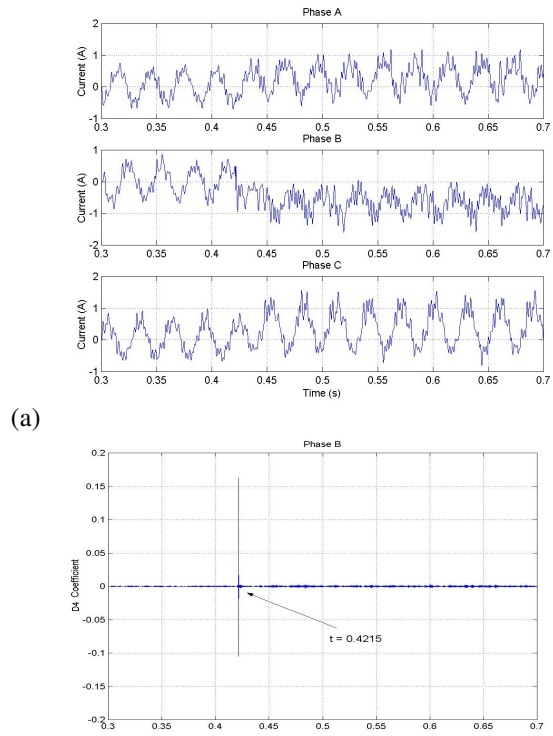
The second fault is the transistor intermittent fault. In this test, the transistor intermittent fault is introduced in the inverter circuit by suppress the firing pulse to the transistor for a short period of time. Figure 7-9 show the phase currents when the intermittent fault of T1, T2



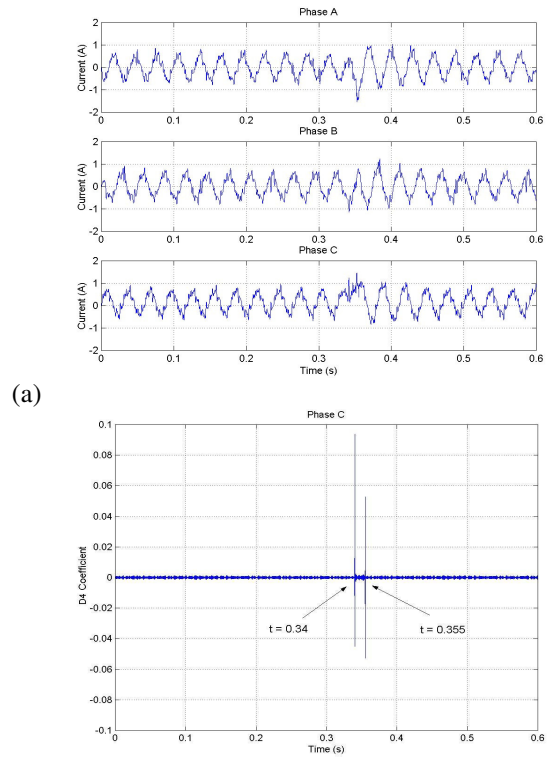
(a) (b)  
 Fig. 5: The experimental result of transistor T2 open-circuit fault. (a) Stator current waveforms during transient, (b) The D4 coefficient of phase C



(a) (b)  
 Fig. 7: The experimental result of transistor T1 intermittent misfiring fault. (a) Stator current waveforms during transient, (b) The D4 coefficient of phase A



(a) (b)  
 Fig. 6: The experimental result of transistor T3 open-circuit fault. (a) Stator current waveforms during transient, (b) The D4 coefficient of phase B



(a) (b)  
 Fig. 8: The experimental result of transistor T2 intermittent misfiring fault. (a) Stator current waveforms during transient, (b) The D4 coefficient of phase C

Table 2: Dc offset reading for one set of experimental results

| Type of fault              | 1st. Reading |         |         | 2nd. Reading |         |         |
|----------------------------|--------------|---------|---------|--------------|---------|---------|
|                            | Phase A      | Phase B | Phase C | Phase A      | Phase B | Phase C |
| T1 base drive open-circuit | -0.399       | 0.2644  | 0.1776  | -0.6057      | 0.4029  | 0.2776  |
| T2 base drive open-circuit | -.3846       | -.2564  | 0.6999  | -.3992       | -.3556  | 0.7226  |
| T3 base drive open-circuit | 0.1562       | -.369   | 0.2427  | 0.3159       | -.6283  | 0.3534  |
| T1 intermittent misfiring  | -.5197       | 0.3271  | 0.1866  | 0.0452       | 0.0189  | -.0879  |
| T2 intermittent misfiring  | -.1575       | -.2735  | 0.6042  | -.0026       | -.0186  | 0.0889  |
| T3 intermittent misfiring  | 0.1439       | -.4632  | 0.1297  | -.0790       | -.0063  | -.0789  |

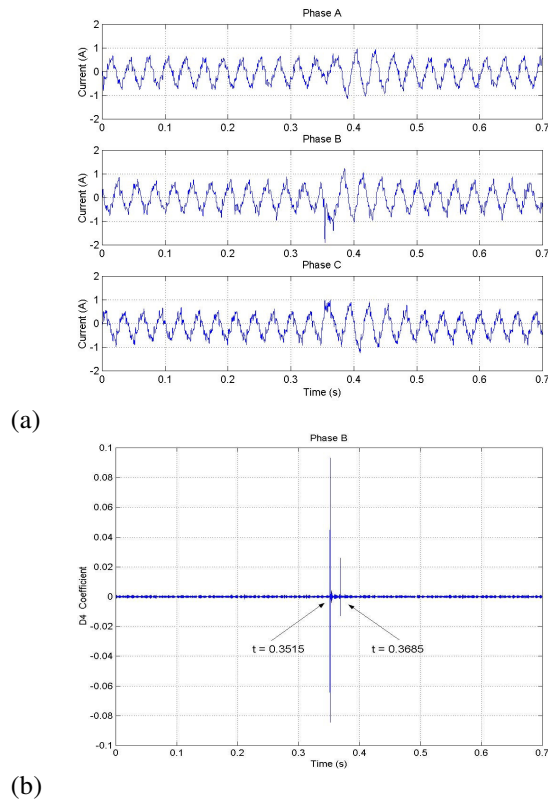


Fig. 9: The experimental result of transistor T3 intermittent misfiring fault. (a) Stator current waveforms during transient, (b) The D4 coefficient of phase B

and T3 occurred, respectively. It can be seen that the system is able to recover from the disturbance and the phase current distortion decays in few output cycles under the effect of the fuzzy logic controller. These results are agreed with the experiment results mentioned in<sup>[9]</sup>. Again, the DWT coefficient is successfully detect the intermittent misfiring fault. In addition, by observing the D4 coefficient, the instant when the fault started and vanished can be obtained. This information is very useful for condition monitoring and maintenance work.

Once the fault is detected by the DWT, the system will start to calculate the currents dc offset. Then, the dc offset value and the polarity will be fed to fuzzy logic system to determine the type of fault. The value and the polarity of dc offset for faulty conditions, are given in

Table 2. The 1<sup>st</sup>. reading is taken just after the fault is detected, while the 2<sup>nd</sup>. reading is taken 5 cycles after the 1<sup>st</sup>. reading. The Table 2 shows that the proposed fault identifier algorithm is agreed with the experimental results. In this project, if the dc offset magnitude is less than 0.1, it will be considered as a healthy condition.

### CONCLUSION

Safety, reliability, efficiency and performance are some of the major issues and concerns for the motor drive system applications. With factors such as aging systems, high reliability demands and cost competitiveness, the issues of preventive and condition-based maintenance, online-monitoring, system fault detection and diagnosis are of increasing importance. A new approach has been presented to detect the 3-phase VSI faults of closed loop fuzzy controlled induction motor. The features are directly extracted from the wavelet transform of the stator currents. The results clearly show that wavelet analysis together fuzzy logic, offers a great potential for monitoring and diagnosis of power electronic drives.

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