Power Quality Improvement Using a Sliding Mode Control of a Series Active Filter

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Abstract: A sliding mode controller (SMC) for a three-phase series active filter was proposed to compensate voltage unbalances, suppress voltage sags and swells and hence improve the power quality of a three-phase ac system. The voltage unbalance compensation and regulation is only based on the positive sequence component decomposition of the supply voltage that is then adjusted to a rated value and used as the reference voltage for the sliding mode controller. This study also includes compensation algorithm, design equations and circuit design criteria. Simulation results ensure the concept and validity of the proposed control system.

Key words: Sliding mode control, series active filter, power quality improvement, voltage unbalance, voltage sags, voltage swells

INTRODUCTION

The power quality in distribution system, especially voltage quality is very important for both industrialized and developing countries. Computers and sensitive electronic equipment are used in everywhere nowadays. A poor power quality can damage or degrade these equipments. In industry and commercial plant and insufficient power quality can lead to the poor quality of products, interruption of important industrial processes and hence economic losses. The factors that affect the voltage quality are voltage unbalance, voltage sags and swells. Voltage unbalance can occur due to an incomplete transposition of transmission lines, unbalanced loads, open delta transformer connection, disconnected three-phase capacitor bank and the proliferation of nonlinear and large single-phase loads[1]. Voltage unbalance worsens the operation of AC electric machines. The negative sequence component in voltage unbalance causes large transient current that leads to reduction of the net torque, increase in losses and temperature rise[2]. Voltage sags and partial or total collapses of one or more phases are normally caused by faults on adjacent feeders such as phase to ground or phase to phase faults. Voltage swells are caused by power factor correction capacitors and transformer switching. Voltage sags or collapse and voltage swells can temporarily interrupt the operation of electrical machine and equipment.

A number of topologies and algorithm to improve the voltage quality have been presented in the literature. However, most of the proposed controllers are open loop based on three-symmetrical component; zero sequence, negative sequence and positive sequence, decomposition to balance and regulate the voltage. Among these papers are a series active filter power filter which compensates voltage unbalance presented by Moran et al[3], an active line conditioner to balance voltage in a three-phase system presented by Bhavaraju and Enjeti[4], distribution system voltage regulation under fault condition using static series regulator presented by Haddad and Joos[5], etc..

This paper proposes a compensation algorithm using a series active filter associated with the sliding mode controller to compensate voltage unbalance and suppress voltage sags and swells. The proposed control structure is shown in Fig. 1.

It is based on a three-phase PWM voltage source inverter connected in series with the power lines through three single-phase current transformers. Three
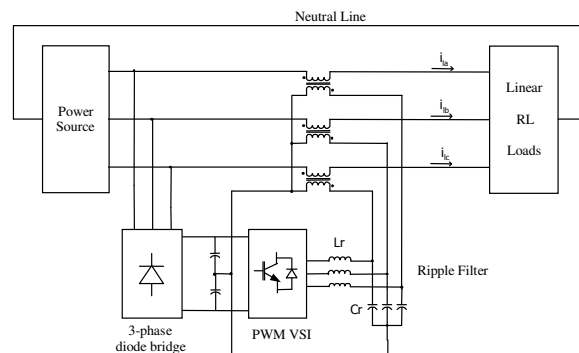

Fig. 1: Control structure of the proposed series active filter

SMCs are employed to track the actual load voltage to the reference voltage. Only the positive sequence component is decomposed from the supply voltage, which is then adjusted to a rated value and used as a reference voltage for the sliding mode controllers. No zero and negative sequence component decompositions are needed in the algorithm; hence, the computational time of the controller is reduced. This leads to the faster response to the transient state of the fault. Furthermore, the proposed algorithm employs a closed loop control system, so the control accuracy and response is much better than the conventional open loop control system.

In the following sections, voltage compensation algorithm, power circuit and simulation results are presented respectively.

VOLTAGE COMPENSATION ALGORITHM

The principle of a voltage compensation is based on the extracting of the positive sequence component from three-phase supply voltages using a transformation given in Eq. 1.

$$v_{a1} = \frac{1}{\sqrt{3}}\left[v_a + \alpha v_b + \alpha^2 v_c \right] \quad (1)$$

where v_a, v_b and v_c represent the phase to neutral source voltages.
v_{a0}, v_{a1} and v_{a2} represent the zero, positive and negative sequence voltage components of phase-a voltage respectively.

$\alpha = e^{j2\pi/3}$ is a phase-shift operator.

It should be noted that the positive sequence of phase-b and phase-c voltages can be calculated from equation similar to Eq. 1. However the results will be merely 120°C phase-shifted from the corresponding components of phase-a voltage. Thus the calculation for the two remaining phases would be unnecessary.

These positive sequence components shall be used to generate reference voltage for the sliding mode controller.

REFERENCE VOLTAGE GENERATION

Let $v_1(t)$ represents an instantaneous positive-sequence voltage with amplitude V_1 and phase angle φ defined by

$$v_1(t) = V_1 \sin(\omega t + \varphi) \quad (2)$$

The amplitude V_1 are calculated from data in a short time window using two samples of the signal $v_1(t)$ as shown below[6].

$$v1 = \frac{[v_{1(k+1)}^2 + v_{1(k)}^2 - 2v_{1(k+1)}v_{1(k)}\cos(\omega T_s)]^{0.5}}{\sin(\omega T_s)} \quad (3)$$

where $v_{1(k+1)}$ and $v_{1(k)}$ represent the positive sequence voltage component at instant $t_{(k+1)}$ and $t_{(k)}$ respectively, T_s is a sampling period equal to $t_{(k+1)}$-$t_{(k)}$.

The reference voltage for the sliding mode controller are calculated as shown in Eq. 4 and 5.

$$v_{rated}(t) = \frac{V_{rated}}{V_1} \times v_1(t) \quad (4)$$

$$\begin{bmatrix} v_{refa} \\ v_{refb} \\ v_{refc} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha^2 & \alpha \\ 1 & \alpha & \alpha^2 \end{bmatrix} \begin{bmatrix} 0 \\ v_{rated} \\ 0 \end{bmatrix} \quad (5)$$

where:
v_{rated} = Rated voltage
v_{rated} = Rated amplitude of load voltage.

SLIDING MODE CONTROLLER

A variable structure control law of SMC is given by

$$u(t) = -\rho\, \text{sgn}(s(t)) \quad (6)$$

or

$$u(t) = \begin{cases} -\rho \text{ if } s(x,x,t) > 0 \\ \rho \text{ if } s(x,x,t) < 0 \end{cases} \quad (7)$$

where:
ρ = Sliding gain
$\text{sgn}(\cdot)$ = Signum or the sign function
The switching function $s(t)$ is defined by

$$s(x,x,t) = e \quad (8)$$

where:
e = Tracking error in the variable = load phase voltage-v_{ref}
The Sliding mode controller block diagram is shown in Fig. 2.

GATING SIGNAL GENERATION

The gating signals of the inverter are generated by comparing the control command, u(t) in Eq. 7 with a triangular waveform whose frequency is kept constant at 6 kHz as shown in Fig. 3.
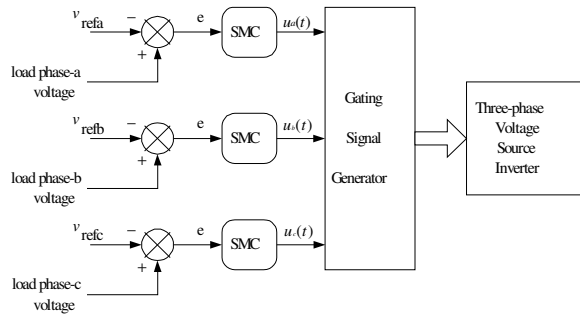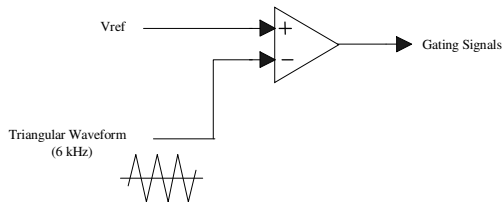
Fig. 2: Sliding mode controller block diagram

Fig. 3: Sliding mode controller block diagram

POWER CIRCUIT DESIGN

In order to quantify the degree of unbalance in the voltages, an unbalance factor must be defined. The unbalance factor, UF is the ratio between the sum of zero sequence and negative sequence voltages $v_0 + v_2$ and the positive sequence voltage v_1.

$$UF = \frac{v_0 + v_2}{v_1} \qquad (9)$$

Similarly, the error between the load voltage and the required rated voltage can be quantified using a magnitude factor. The magnitude factor, MF, is the ratio between the positive sequence voltage and a rated line to line voltage required by loads v_{rated}.

$$MF = \frac{v_1}{v_{rated}} \qquad (10)$$

CURRENT TRANSFORMER (CT)

The purpose of the CT's is not only to isolate the PWM inverter from the power system, but also to match the voltage and current ratings of the PWM inverter with that of the power system.

The maximum secondary voltage of the CT is given by

$$V_{s,max} = \frac{(V_{rated} - V_1) + (V_0 + V_2)}{\sqrt{3}} \qquad (11)$$

which can be written in term of MF and UF as shown below.

$$V_{s,max} = \frac{\left\lfloor 1 - |MF|_{min}\left(1 - |UF|_{max}\right)\right\rfloor \cdot V_{rated}}{\sqrt{3}} \qquad (12)$$

The maximum primary voltage of the CT is given by

$$V_{p,max} = G.V_{dc} \qquad (13)$$

where G is the inverter gain.

The total apparent power rating (VA rating) of each CT, which is 1/3 of the inverter's rating, is given by

$$S_{max}(each\,CT) = V_{s,max}.I_{rated} \qquad (14)$$

where I_{rated} is rated load current.

The turn ratio, a, of the current transformer is selected in accordance with the inverter dc bus voltage, V_{dc} and load rated voltage, V_{rated} as follows.

$$CT\,turn\,ratio(a) = \frac{n_2}{n_1} = \frac{V_{dc}/2}{V_{rated}/\sqrt{3}} \qquad (15)$$

PWM VOLTAGE-SOURCE INVERTER

The rated apparent power required by the inverter can be obtained by computing the apparent power generated in the primaries of the current transformers as illustrated below.

$$S_{max}(inverter) = 3.V_{s,max}.I_{rated} \qquad (16)$$

The inverter switch ratings are defined by the following equations.

$$V_{swpk} = V_{dc}/2 \qquad (17)$$

$$I_{swpk} = \sqrt{2}.\frac{V_{s,max}.I_{rated}}{V_{p,max}} \qquad (18)$$

PASSIVE FILTER TO SUPPRESS SWITCHING RIPPLES

As shown in Fig. 1, the purpose of Lr and Cr connected in the primary of the CT is to suppress the switching voltage ripples caused by the voltage source PWM inverter.
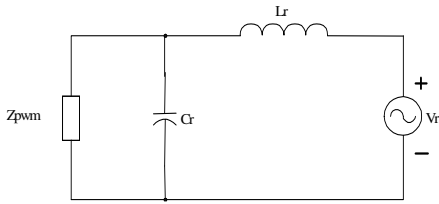
Fig. 4: Equivalent circuit for Vr

Fig. 4 shows the equivalent circuit for the switching voltage ripple Vr.

Zpwm is the amplitude of Zs (source impedance), which is seen from the primary of the CT and can be represented as

$$Z_{pwm} = \left(\frac{n_1}{n_2}\right)^2 |Z_s| \qquad (19)$$

At the frequency of the triangular waveform, the following relation between the ripple filter parameters has to be satisfied.

$$X_{crf} = \langle\!\langle X_{lrf} \langle\!\langle Z_{pwm} \qquad (20)$$

where X_{crf} and X_{lrf} are the capacitive and inductive reactance of the ripple filter respectively.

The design criteria for X_{crf} and X_{lrf} is such that the voltage drop in the inductor at the ripple frequency must be larger than the voltage drop in the capacitor, however for the frequency that needs to be compensated, the voltage drop in the capacitor must be larger than the voltage drop in the inductor[6].

SIMULATION RESULTS

The proposed series active filter has been verified by simulation. The results are divided into 5 categories according to the arbitrary imposed supply conditions, as shown in Fig. 5-9. In each case, the compensator begins to operate at 40 ms.

Case 1: Balance voltage sags with |MF| = 0.65
Case 2: Balance voltage swells with |MF| = 1.35
Case 3: Unbalance voltage sags with |UF| = 0.261 and |MF| = 0.516
Case 4: Unbalance voltage swells with |UF| = 0.144 and |MF| = 1.20
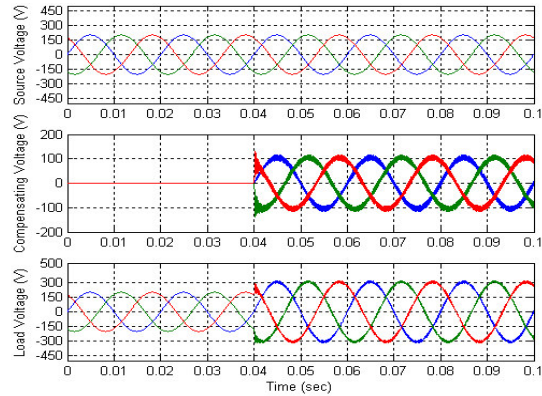**Case 5:** 1-phase loss with |UF| = 0.552 and |MF| = 0.766

Fig. 5: Case 1: Load phase voltage, compensating voltage and source phase voltage in case of balance voltage sags with |MF| = 0.65
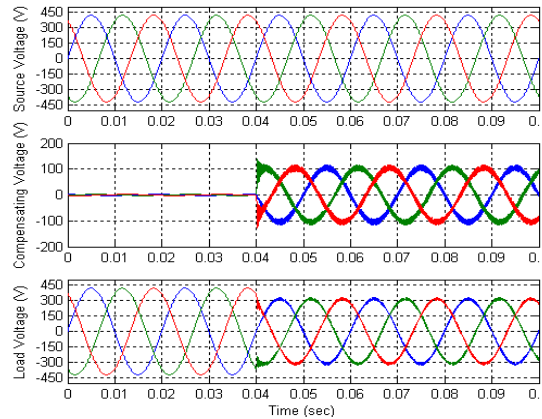

Fig. 6: Case 2: Load phase voltage, compensating voltage and source phase voltage in case of balance voltage swells with |MF| = 1.35
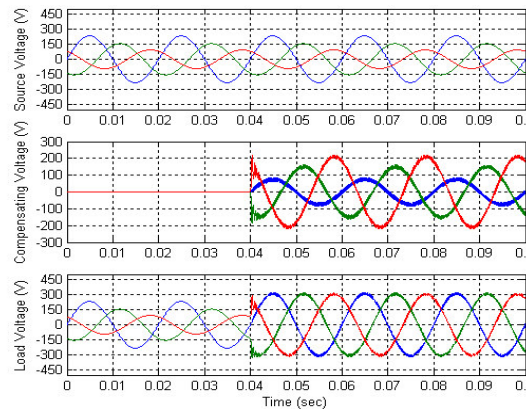

Fig. 7: Case3: Load phase voltage, compensating voltage and source phase voltage in case of
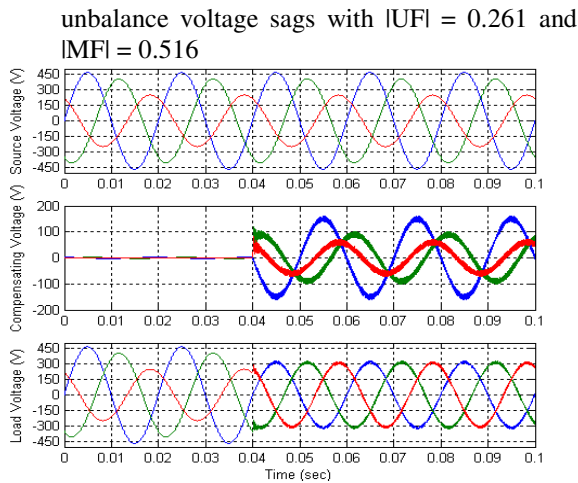
unbalance voltage sags with |UF| = 0.261 and |MF| = 0.516

Fig. 8: Case 4: Load phase voltage, compensating voltage and source phase voltage in case of unbalance voltage swells with |UF| = 0.144 and |MF| = 1.20
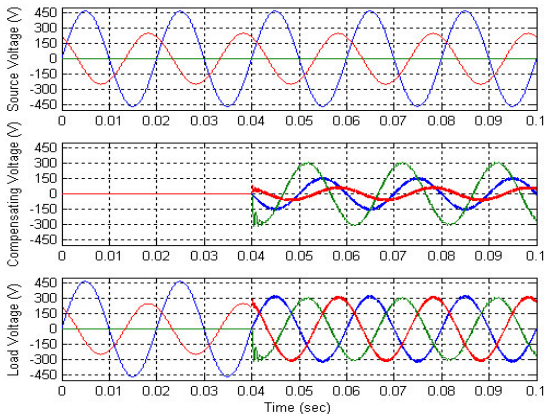

Fig. 9: Case 5: Load phase voltage, compensating voltage and source phase voltage in case of 1-phase loss with |UF| = 0.552 and |MF| = 0.766

CONCLUSION

This study has shown the feasibility and compensation capability of a three-phase series active filter (SAF) with sliding mode controller. The SAF based on a three-phase voltage source inverter connected in series to the supply through transformers. The SMC, of which the control structure is simple and easily to apply was employed to track the load voltage to the reference voltage. Its performance is very good in term of the control accuracy and response. The proposed SAF can compensate voltage unbalance, sags and swells and hence improve the power quality of the electrical distribution system. Voltage balancing and regulation was successfully done without zero and negative sequence component decomposition. This reduces the computational time of the controller and leads to a fast response to the system transience. The simulation results show a very good performance of the proposed SAF configuration and control scheme.

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